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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/632,176	07/31/2003	Farrokh Ayazi	062020-1440	9833

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EXAMINER	
KANG, DONGHEE	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 11/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/632,176	AYAZI ET AL.	
	Examiner	Art Unit	
	Donghee Kang	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) *10-17 and 29-35* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9 and 18-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/14 & 6/13, 2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of Group I (claims 1-9 & 18-28) in the reply filed on September 13, 2004 is acknowledged.

The traversal is on the ground(s) that the invention must be independent or distinct and there is no significant burden on the examiner and certainly no serious burden required by MPEP section 803. This is not found persuasive.

A restriction requirement between one set of product claims and a set of process claims was issued in the Office Action of paper No.8, mailed on 10 August 2004. "Section 121 [of Title 35 USC] permits a restriction for 'independent and distinct inventions', which the PTO construes to mean that the sets of claims must be drawn to separately patentable inventions." See Applied Materials Inc. v. Advanced Semiconductor Materials 40 USPQ2d 1481, 1492 (Fed. Cir. 1996) (Archer, C.J., concurring in-part and dissenting in-part). A product and the process of making the product are "two independent, albeit related invention." See In re Taylor, 149 USPQ 615, 617 (CCPA 1966). "When two sets of claims filed in the same application are patentably distinct or represent independent inventions, the examiner is to issue a restriction requirement." See In re Berg, 46 USPQ2d 1226, 1233 n. 10 (Fed. Cir. 1998).

The examiner, in issuing a restriction requirement, must demonstrate "one way distinctiveness." Applied Materials Inc. at 1492. As stated within the restriction requirement, "inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product

or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f))." In this application, the examiner restricted the product claims from the process claims on the grounds that "the product as claimed can be made by another and materially different process such as a forming an oxide layer using growing instead of coating and that, as a result, a restriction was necessary.

In addition to one way distinctiveness, the examiner must show "why it would be a burden to examine both sets of claims." Applied Materials Inc. at 1492. "A serious burden on the examiner may be prima facie shown if the examiner shows by appropriate explanation either separate classification, separate status in the art, or a different field of search." MPEP 803. An explanation was provided in the restriction requirement is proper because the product claims and the process claims "have acquired a separate status in the art."

The criteria of distinctness and burdensomeness have been met, as demonstrated hereinabove. Applicant has set out no other specific reason, therefore restriction requirement is maintained. Accordingly, the requirement is still deemed proper and is therefore made FINAL.

Information Disclosure Statement

2. Acknowledgment is made of receipt of applicant's Information Disclosure Statement (PTO-1449) field May 14 & June 03, 2004.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Ayazi et al. (High Aspect-Ratio Combined Poly and single-crystal Silicon (HARPSS) MEMS Technology, J. of Micro. Sys., Vol.9, No.3, September 2000).

Re claim 1, Ayazi et al. teach a method for fabricating micro-electro-mechanical system (MEMS) capacitive resonators, the method comprising (Fig.2):

Forming trenches in a substrate; conformally coating the substrate with an oxide; filling the coated trenches with polysilicon; patterning the polysilicon; releasing a resonator structure derived from the substrate; and removing the conformally coated oxide. See section **II. Fabrication Technology**.

Re claim 2, Ayazi et al. teach the method further comprising:

Depositing nitride on at least one of an insulating layer and the substrate; patterning the nitride to isolate pads; providing polysilicon to the patterned pads; and metallizing the pads.

Re claim 3, Ayazi et al. teach the releasing comprising separating the resonating structure from the polysilicon.

Re claim 4, Ayazi et al. teach the releasing comprises an isotropic silicon etching of the resonator.

Re claim 5, Ayazi et al. teach the filling includes filling out from sidewalls of the trenches.

Re claim 6, Ayazi et al. teach the removing includes forming a gap between the resonator structure and the polysilicon in a self-aligned manner.

Re claim 7, Ayazi et al. teach the gap is approximately less than 90 nanometers. See section C. Various size air gap in page 291.

Re claim 8, Ayazi et al. teach the filling includes forming an electrode.

Re claim 9, Ayazi et al. teach the etching includes forming high-aspect ratio trenches.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 18-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ayazi et al. (High Aspect-Ratio Combined Poly and single-crystal Silicon (HARPSS) MEMS Technology, J. of Micro. Sys., Vol.9, No.3, September 2000) in view of Lin et al. (US 6,413,793).

Re claim 18, Ayazi et al. teach a method for fabricating micro-electro-mechanical system (MEMS) capacitive resonators, the method comprising (Fig.2):

Forming trenches in a semiconductor substrate; confromally coating the semiconductor substrate with an oxide; filling the coated trenches with polysilicon, wherein electrode are derived from the polysilicon; forming release openings; and removing the conformally coated oxide and an oxide of the semiconductor substrate,

wherein a capacitive gap is formed, wherein a resonating element of the capacitive resonator is released.

Ayazi et al. do not explicitly teach the semiconductor-on-insulator (SOI) substrate. However, Lin et al. noted that microstructure are often formed silicon-on-insulator (SOI) structures. Forming microstructures on SOI structures provides significant advantages, such as superior electrical isolation between adjacent components, reducing of integrated circuit capacitance, and lower operating voltages. See Col.1, line 60 – Col.2, line 3.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form MEMS resonator of Ayazi on SOI structure as taught by Lin since SOI structures provides significant advantages, such as superior electrical isolation between adjacent components, reducing of integrated circuit capacitance, and lower operating voltages.

Re claim 19, Ayazi et al. as modified by Lin teach the method further including:

Growing and patterning an insulator oxide (paragraph 2, on page 289), wherein the insulator oxide provides isolation between the semiconductor substrate and wire-bonding pads; depositing and patterning nitride, wherein the nitride provides protection for the insulator oxide disposed on the pads; growing and removing a surface treatment oxide, wherein the surface treatment oxide enables the reduction of the roughness of sidewalls of the resonating element; depositing polysilicon to form the wirebonding pads for drive and sense electrode; metallizing the pads; and patterning the polysilicon inside the trenches.

Re claim 20, Ayazi et al. as modified by Lin teach the forming release opening comprises anisotropically etching to an oxide layer of the SOI structure, such that the undercut of the resonating element is facilitated.

Re claim 21, Ayazi et al. as modified by Lin teach the filling includes one of filling the trenches with doped LPCVD polysilicon such that the electrodes are formed vertically and depositing and patterning doped LPCVD polysilicon.

Re claim 22, Ayazi et al. as modified by Lin teach the forming trenches includes one of deep reactive ion etching and regular reactive ion etching to an oxide layer of the SOI substrate.

Re claim 23, Ayazi et al. as modified by Lin teach the conformally coating include depositing a LPCVD high-temperature oxide of approximately less than 100 nanometers.

Re claim 24, Ayazi et al. as modified by Lin teach the conformally coating is scalable to correspond to a desired thickness of a lateral gap spacing for the capacitive resonator (see page 291 "various size of air gap").

Re claim 25, Ayazi et al. as modified by Lin teach the removing comprises an anisotropic plasma etching such that at least a portion of the oxide remains on sidewalls of the resonating element.

Re claim 26, Ayazi et al. as modified by Lin teach the releasing comprises exposing the SOI substrate to a solution $HF:H_2O$ to release the resonating element from a handle layer and the electrodes.

Re claim 27, Ayazi et al. as modified by Lin teach the forming trenches includes etching high-aspect ratio trenches.

Re claim 28, Ayazi et al. as modified by Lin teach the removing includes forming a gap between the resonating element and the polysilicon in a self-aligned manner.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Donghee Kang whose telephone number is 571-272-1656. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Donghee Kang, Ph.D.
Primary Examiner
Art Unit 2811

dhk